CLAIMS

What is claimed is:

1. A system for interconnecting two or more computer bus architectures, comprising:

a first bus segment to transmit data information;

a first half bridge circuit connected to said first bus segment;

a second bus segment to transmit data information;

a second half bridge circuit connected to said first half bridge circuit and said second bus segment for transferring data information between said first half bridge circuit and said second bus segment.

2. The system for interconnecting two or more computer bus architectures according to claim 1, wherein:

said first bus segment is a PCI architecture bus.

3. The system for interconnecting two or more computer bus architectures according to claim 1, wherein:

said second bus segment is a PCI architecture bus.

4. The system for interconnecting two or more computer bus architectures according to claim 1, wherein:

said first half bridge segment and said second half bridge segment communicate with a high speed serial bus protocol.

5. The system for interconnecting two or more computer bus architectures according to claim 1, wherein:

said first bus segment operates at a different bus frequency than a bus frequency of said second bus segment.

6. The system for interconnecting two or more computer bus architectures according to claim 1, wherein:

said first bus segment operates at a substantially same bus frequency as a bus frequency of said second bus segment.

7. The system for interconnecting two or more computer bus architectures according to claim 1, wherein:

at least one of said first half bridge circuit and said second half bridge circuit are field programmable.

8. The system for interconnecting two or more computer bus architectures according to claim 1, wherein:

said first half bridge circuit and said second half bridge circuit recover a clock signal from, respectively said first bus segment and said second bus segment.

9. The system for interconnecting two or more computer bus architectures according to claim 4, wherein:

said high speed serial bus protocol is full duplex.

10. A method of interconnecting two or more computer bus architectures comprising:

connecting a first half bridge circuit to a first bus segment;

connecting said first half bridge circuit to a second bus segment; and

transmitting data information from said first half bridge circuit over said second bus segment.

11. A method for interconnecting two or more computer bus architectures according to claim 10, wherein:

said step of transmitting data transmits data over a PCI architecture bus.

12. A method for interconnecting two or more computer bus architectures according to claim 10, wherein:

said step of transmitting data transmits data over a PCI architecture bus.

13. A method for interconnecting two or more computer bus architectures according to claim 10, wherein:

communication over said first half bridge segment and said second half bridge segment occurs with a high speed serial bus protocol.

14. A method for interconnecting two or more computer bus architectures according to claim 10, wherein:

operation of a bus frequency of said first bus segment is different than a bus frequency of said second bus segment.

15. A method for interconnecting two or more computer bus architectures according to claim 10, wherein:

operation of a bus frequency of said first bus segment is substantially the same as a bus frequency of said second bus segment.

16. A method for interconnecting two or more computer bus architectures according to claim 10, further comprising:

field programming at least one of said first half bridge circuit and said second half bridge circuit.

17. A method for interconnecting two or more computer bus architectures according to claim 10, further comprising:

recovering a clock signal for said first half bridge circuit and said second half bridge circuit from their respectively connected said first bus segment and said second bus segment.

18. A method for interconnecting two or more computer bus architectures according to claim 13, wherein:

full duplexing said high speed serial bus.

19. A system for interconnecting two or more computer bus architectures comprising:

a first half bridge circuit means connected to a first bus segment means;

a second half bridge circuit means connected to a second bus segment means; and

a second bus segment means transmitting data information from said first half bridge circuit over said second bus segment.

20. The system for interconnecting two or more computer bus architectures according to claim 19, wherein:

said first bus segment is a PCI architecture bus.

21. The system for interconnecting two or more computer bus architectures according to claim 19, wherein:

said second bus segment means is a PCI architecture bus.

22. The system for interconnecting two or more computer bus architectures according to claim 19, wherein:

said first half bridge segment means and said second half bridge segment means communicate with a high speed serial bus protocol.

23. The system for interconnecting two or more computer bus architectures according to claim 19, wherein:

said first bus segment means bus frequency is different than said second bus segment means bus frequency.

24. The system for interconnecting two or more computer bus architectures according to claim 19, wherein:

said first bus segment means bus frequency is the same as said second bus segment means bus frequency.

25. The system for interconnecting two or more computer bus architectures according to claim 19, further comprising:

at least one of said first half bridge circuit means and said second half bridge circuit means are field programmable.

26. The system for interconnecting two or more computer bus architectures according to claim 19, further comprising:

said first half bridge circuit means and said second half bridge circuit means recover a clock signal from their respectively connected said first bus segment means and said second bus segment means.

27. The system for interconnecting two or more computer bus architectures according to claim 23, wherein:

said high speed serial bus protocol is full duplex.